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A compact drain current model based on Genetic algorithm computation to study the nanoscale Double-Gate MOSFETs

T. Bendib[1], F. Djeffal[1,*], M. Maguellati[1], A. Benhaya[1] and M. Chahdi[2]
[1] LEA, Department of Electronics, University of Batna 05000, Algeria
[2] LEPCM, Department of Physics, University of Batna 05000, Algeria
[*] Corresponding author
Fax: 002313924540, Tel: 00213773796503
E-mail: djeffaldzdz@yahoo.fr

Abstract. Simulations tools thath can be applied to design nanoscale transistors in the future require a new theory and modeling techniques, which capture physics of quantum transport accurately and efficiently. In this paper, we apply the Genetic algorithm technique to study nanoscale Double-Gate MOSFETs. The developed model is particularly well-adapted to ultra-scale devices with short channel lengths and ultra-thin silicon films. Extracted parameter values reproduce *I-V* characteristics within 7 % RMS error for wide range of gate lengths.

Keywords:.

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1. Introduction

The symmetric Double-Gate (DG) MOSFET shown in Fig. 1 has been considered as one of the most promising candidates for the sub-50 nm regime in CMOS scaling with the following advantages: 1) light doping of the channel reducing the mobility degradation due to elimination of impurity scattering; 2) good control of short channel effects; 3) ideal subthreshold slope due to elimination of substrate doping [1-4].

Previous works on DG MOSFET include fabrication procedures, analytical modeling and numerical analysis [1-6]. To extract information accurately about the *I-V* characteristics requires the solution of Schrödinger and Poisson equations based on the non-equilibrium Greens function (NEGF) formalism, assuming QM effects are to be fully accounted. But from the circuit modeling point of view even 2-D solution of numerical NEGF is an overkill approach in term of both complexity and computational cost. For analytical modeling, in general, it is difficult or almost impossible to obtain closed form analytical models for nanoscale DG-MOSFETs [3]. Thus, models are obtained by a simplification of the full physical model [3]. Model accuracy and simplicity is important for the design of complex circuits. Genetic algorithm (GA) based models would be preferable and could provide practical solutions. We call this type of solution approach as intelligent simulators [3].

In this paper, we present the applicability of genetic algorithm to optimize an analytical drain current model in order to study the DG MOSFET in nanoscale regime. The database used for the optimization of our analytical model is built on the basis of a numerical model of the current-voltage characteristics of a DG MOSFET developed using the NEGF formalism [2, 3, 7]. The optimized compact model obtained from this study can be used as the interface between device modeling and circuit simulators in order to analyze the downscaling of DG MOSFETs for nanoscale digital and analog applications. A simplified overview is shown in Fig. 2.

2. Genetic algorithm computation

Genetic algorithm based methods have been widely used for optimizing various complex and nonlinear processes (controller design, stage forecasting, parameter estimation, etc.). In GA, variables of a problem are represented as genes in a chromosome, and the chromosomes (population) are evaluated according to their fitness values. Given a random initial population GA operates in cycles called generations. The problem to be solved is defined in terms of an evaluation function (fitness function), which is used to evaluate the chromosomes. A chromosome evaluated as having a high fitness value is likely to be a good solution of the problem.

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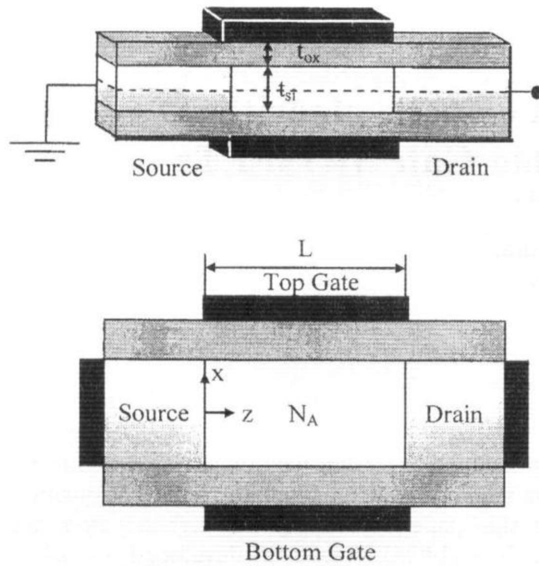

Fig. 1. The ultra-thin DG MOSFET structure used in this study with channel doping $N_A = 10^{16}$ cm^{-3}, silicon thickness $t_{Si} = 3$ nm and oxide thickness $t_{ox} = 1.5$ nm.

Implementation of GA requires determination of six fundamental issues: chromosome representation, selection function, the genetic operators, initialization, termination and evaluation function [8, 9]. In this study, the model parameters (about 15 parameters) are treated as the GA chromosome and the fitness function is defined in terms of the quality of fit for numerical data (NEGF simulations).

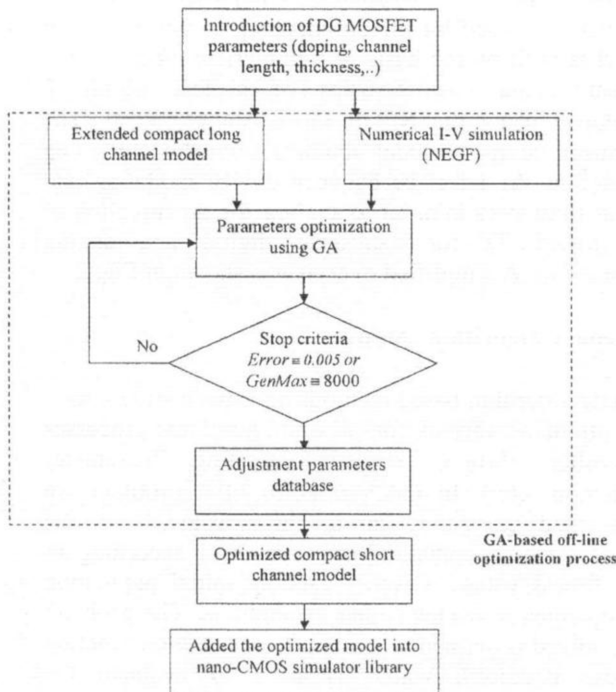

Fig. 2. A computational flowchart for the simulation based evolutionary approach to the study of the nanoscale CMOS circuits.

The objective in the design of optimal *I-V* curves is to find the configuration of model parameters for compact device model that satisfies the features of the numerical or measured *I-V* characteristics. In DG MOSFET device simulation, the relationship between modeling input parameters and computed results can be given as:

$$I_{ds} = h(V_{gs}, V_{ds}, \vec{C}) \tag{1}$$

where V_{gs}, V_{ds} are input bias voltage represent the gate-source voltage and the drain-source voltage respectively, and vector $\vec{C}$ is the vector of construction parameters for compact model, which will be optimized to fit the numerical results using GA technique.

Basing on the compact model of long channel DG MOSFET developed in [10] and mobility model [11], we can define a new adjusted (extended) compact model given as

$$I_{ds} = \left(\frac{\mu_{\text{eff}}}{L}\right)\left[\frac{q_s^2 - q_d^2}{2n_1} + (q_s - q_d)\right](1 + \text{mob}9V_{ds}) \tag{2a}$$

with $n_1 = 1 + \text{sub}_1\left(\frac{C_{\text{si}}}{C_{\text{si}} + C_{\text{ox}}}\right)$ represents the ideality factor, q_s and q_d are the normalized charge at the source and the drain, respectively, C_{si} and C_{ox} represent the silicon and oxide capacitance, respectively, and μ_{eff} represents the effective mobility given [11] as

$$\mu_{\text{eff}} = \left(\frac{\mu_T}{\left[1 + \mu_T E / v\text{sat}\right]^{\text{mob}_6}}\right)^{\frac{1}{\text{mob}_6}} \tag{2b}$$

with $\mu_T = \text{mob}_1 + \left(\frac{\text{mob}_1.(T/300)^{\text{mob}_3} - \text{mob}_2}{1 + (N_A/\text{mob}_5)^{\text{mob}_4}}\right)$ and

$v\text{sat} = \text{mob}_7\sqrt{\tanh\left(\frac{\text{mob}_8}{T}\right)}$.

The analytical expression of the normalized charge within the channel is given in [10] as

$$q_l = \text{sub}_2 n_1 \ln\left(1 + \exp\left(\text{sub}_3.V_{gs} - \left(\frac{V_{to}}{n_1}\right) - V_{\text{ch}}\right)\right) \tag{2c}$$

where ln is the natural logarithm, V_{to} and V_{ch} represent the threshold and channel voltage, respectively. The threshold voltage can be obtained from the integration constant [10] as

$$V_{to} = \text{th}_1 V_{fb} + \text{th}_2\left(\frac{C_{\text{eq}}}{C_{\text{ox}}}\right)V_{fb} + \\ + \text{th}_3.\left(\frac{C_{\text{eq}}}{C_{\text{ox}}}\right)2\phi_B + \text{th}_4\left(1 + \left(\frac{C_{\text{eq}}}{C_{\text{si}}}\right)\right).\left(\frac{qN_A t_{\text{si}}}{C_{\text{ox}}}\right) \tag{2d}$$

with $C_{\text{eq}} = \frac{C_{\text{si}}.C_{\text{ox}}}{C_{\text{si}} + C_{\text{ox}}}$, and ϕ_B, V_{fb} are the barrier and the flat band voltage, respectively. By replacing V_{ch} with the S/D voltage, q_s and q_d can be evaluated. Using the

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expressions (2a) and (2c), the analytical *I-V* characteristics of the long channel DG MOSFET can be calculated.

The coefficients sub_i $(i = 1:3)$, th_i $(i = 1:4)$ and mob_i $(i = 1:9)$ represent the adjustment parameters (elements of the vector $\vec{C}$) that will be optimized in order to develop our short channel compact model to study the scaling capability of the DG MOSFETs. In compact drain current models, device performances are highly interdependent through the drain current. Here, model parameters are separated into three groups (threshold group, subthreshold and mobility groups). Unfortunately, these three groups of parameters cannot be extracted independently, and interdependently determine the *I-V* characteristics. Therefore, extraction of parameters has to be performed in principle with all the parameters simultaneously for all bias conditions.

The fitness function f used for evaluation of the chromosomes, the adjustment of parameters, is defined as:

$$f = \frac{1}{M}\sum_{V_{gs}}\sum_{V_{ds}}\left[\frac{I_{ds,NUM} - I_{ds,GA}}{I_{ds,NUM}}\right]^2 + \\ + \frac{1}{M}\sum_{V_{gs}}\sum_{V_{ds}}\left[\frac{\log(I_{ds,NUM}) - \log(I_{ds,GA})}{\log(I_{ds,NUM})}\right]^2, \tag{3}$$

where M represents the total number of target data points, the subscript *'NUM'* and *'GA'* indicate numerical data (NEGF) and calculated data by GA technique, respectively.

3. Results and discussions

For the implementation of the GA, tournament selection is employed which selects each parent by choosing individuals at random, and then choosing the best individual out of that set to be a parent. Scattered crossover creates a random binary vector. It then selects the genes where the vector is unity from the first parent, and the genes where the vector is zero from the second parent, and combines the genes to form the child. An optimization process was performed for 50 population size and maximum number of generations equal to 8000, for which stabilization of the fitness function was obtained. GA parameters were varied and the associated optimization error was recorded (Table 1). For this configuration, the fitness function was 0.0006 and almost 100 % of the submitted cases were learnt correctly. This resulted in 400 000 parameter set evaluations, and took about 2 hours to complete using Windows XP with Pentium IV (1.5 GHz). In order to validate the predictive property of the optimized population, the numerical set was compared to the GA optimized compact current model. Fig. 3 shows that a good agreement between numerical and predicted results was found. Hence, the optimized compact model can be used to predict other combinations of input variables (V_{gs}, V_{ds}, L, *etc.*) in full range. This last observation shows the applicability of GA technique to study the nanoscale DG MOSFETs basing on long channel compact current model. The optimized parameters of the short channel compact current model found in this study are shown in Table. 2.

Fig. 4 presents comparisons between target data (NEGF) and model data calculated with the model parameters extracted by our GA for the short channel DG MOSFET. We can see that proposed model provide a good agreement for a very wide interval of geometrical and physical parameters for DG MOSFETs in comparison with numerical simulation. Table 3 summarizes the normalised RMS (Rout Mean Square) for *I-V* characteristics. For all the device lengths, the RMS errors are within 7 %.

Table 1. Parameters used for GA computation.

GA parameters	Values
Population size	50
Maximum number of generations	8000
Fitness scaling	Proportional
Selection	Tournament
Crossover	Scattered
Mutation	Gaussian distribution

Table 2. Fitting parameters obtained from our optimization (L = 30 nm).

Subthreshold group
sub_1= 0.10312177836895, sub_2= 0.496832466125488, sub_3= 0.990412968546536
Threshold group
th_1= 0.398703214076887, th_2= 0.042422093451023, th_3= 1.186765499701093, th_4= 0.030267874633365,
Mobility group
mob_1 = 51.2557946145534, mob_2 = 1321.042391657829, mob_3 =1.578610211610794, mob_4 = 0.911914846301079, mob_5 = 4.00757680802057 E16, mob_6 = 2.720140933990478, mob_7 = 1.1827376365661621 E9, mob_8= 100.06791114807129, mob_9= 0.129484132295987

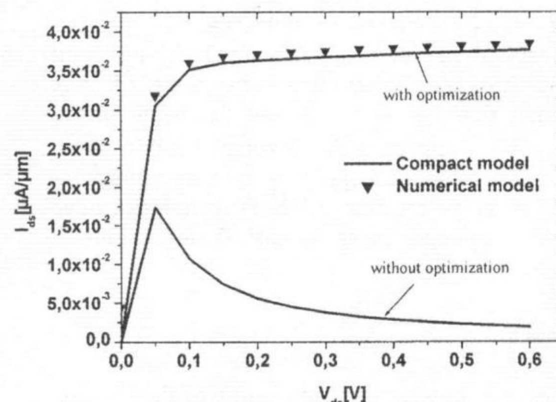

Fig. 3. Numerical and compact drain current models vs. drain voltage for DG MOSFET (L = 30 nm, V_{gs} = 0.3 V).

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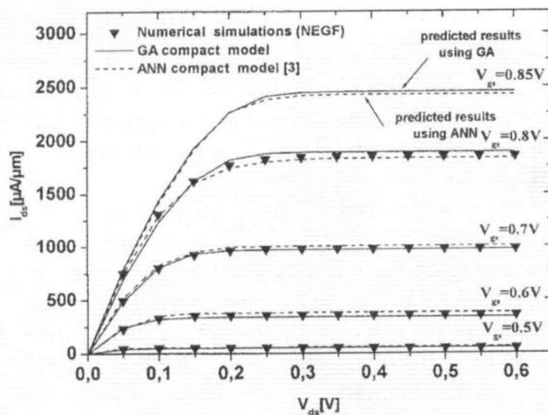

Fig. 4. Numerical (symbols) and simulated (solid and dashed lines) drain current vs. drain voltage for DG MOSFET (L = 30 nm).

Table 3. Calculated fitting errors of *I-V* characteristics for different channel lengths.

L (nm)	20	25	30	35	40	45	50
RMS %)	6.82	2.99	1.52	1.05	0.78	0.65	0.57

Table 4. Comparison between the various approaches of modeling of the nano-DG.

	Model	Effectiveness of the approach
GA-based approach	Analytical approach	Accurate and speed
ANN-based approach [3]	Black-box (matrix of weights)	Accurate and speed
Numerical model (NEGF)	Numerical approach	Accurate and very slow
Analytical model	Analytical approach	Less accurate and speed

The forgoing results show that the GA-based model makes it feasible to include quantum effects accurately and generally in nanoelectronic device simulation. In order to show a comparison between the GA-based computation and ANN-based approach [3] in the field of nano-CMOS circuits simulation, Table 4 shows that the neural method is a behavioural approach of modeling where the neural model is given as a black-box and defined by 3 different blocks: input vector-weight matrix and activation function-output vector. Contrary, in the case of GA-based approach the developed model is an analytical expression that includes additional adjustment parameters. It is to note that the both techniques have shown a good agreement with numerical simulations as it can be seen from Fig. 4.

4. Conclusion

In this paper, we showed the applicability of the Genetic algorithm technique to the simulation problem of nanoscale CMOS circuits. 2-D numerical non-equilibrium Green's function (NEGF) formalism simulation is used to optimize our compact model. After optimization, the extracted parameters by GA are imported into the long channel DG MOSFETs model in order to develop our short channel DG MOSFETs compact model. The encouraging comparisons between 2-D numerical results and optimized compact model simulations have indicated that the developed approach particularly suitable to be incorporated in electronic devices simulators for nanoscale CMOS circuit simulation.

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